# Lab 3 Behavioral Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? \_yes\_\_

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here. Otherwise write “n/a”: **\_n/a\_\_\_**

Student Name: Chris Cyr  
Student ID: 12436037  
Date Completed: 5/20/22  
Time Spent: Reviewing Digital Design Material: 30min  
 Design/Preparation Work: 2hr  
 VHDL Coding & Debugging: 6hr

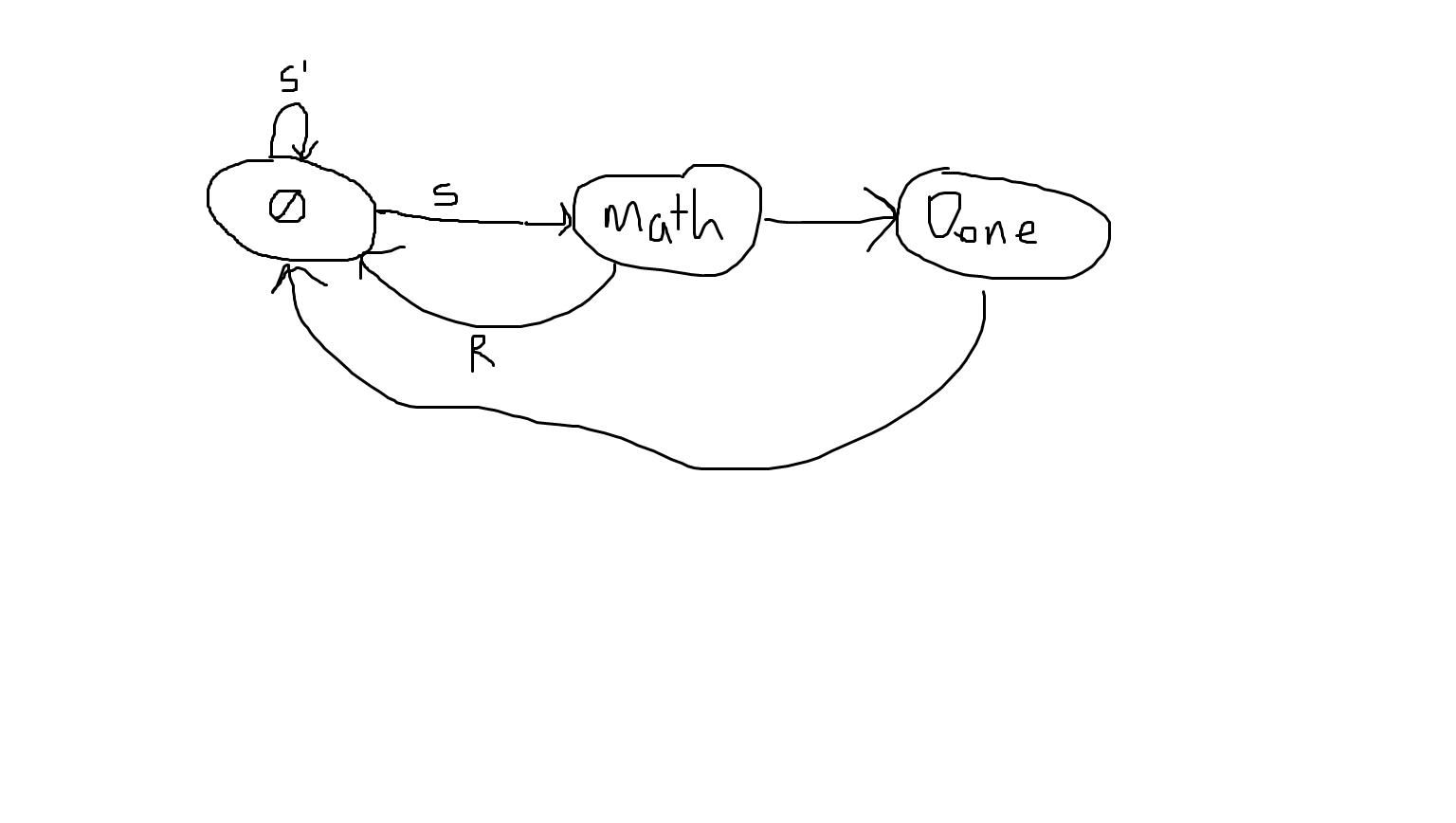
## Behavioral Overview

What % do you feel you completed on the lab? Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

\_\_100%\_\_

## Lab 3 FSMD

Show your FSMD for Lab 3 here. You can use Visio, another UML Diagramming tool, or attach a picture of your FSM as long as it is legible. If you attach a picture, ensure it is the correct orientation. Be sure to show what computations you want to complete in each step of your FSMD for your behavior. Make sure inputs/outputs are clearly identified.



## Lab 3 Behavioral Simulation Graph

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

